Modification of Surface Properties of Silicon Wafers by Laser-Assisted Electrochemical Etching

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Abstract. In this paper, the structural properties of porous silicon layer PSL are reported. Photo-assisted (laser) electrochemical etching PECE technique used to fabrication PSL from n-type wafer silicon as a function of etching time. Optical microscopy image confirmed that the surface topography of porous silicon layer formation was a mud-like structure. The porosity and thickness have been determined gravimetrically are varied from 61% to 82% and 7.2 μm to 9.4μm respectively. The XRD patterns show that one diffraction peak for all PSL through anodization duration and it is assigned to the (400) plane and data confirmed the porous silicon PS was nanocrystalline.

Introduction

The strong visible light emission in porous silicon is quite surprising and such structure can exhibit a large variety of morphologies and particles sizes [1]. Porous silicon PS is formed in HF-based electrolytes ensuring local pit-like electro-dissolution of silicon. This material attracts much attention due to emerging applications in electronics, optics, and chemistry [2]. The physical properties of porous silicon depend strongly on the preparation method and related parameters like etching solution, etching time, potential etc. [3]. All the properties of PS, such as porosity, thickness, pore diameter and microstructure, depend on anodization conditions. These conditions include HF concentration, current density, wafer type and resistivity, anodization duration, illumination (n-type mainly), temperature, ambient humidity and drying conditions [4]. The properties of PS are intimately related to its morphology, and much attention was given to control the morphology of PS by changing the anodization parameters [5]. Many of the previous studies of the structure have been carried out on porous silicon layer under a wide range of conditions for the preparation of the electrochemical etching. This work has been performed at a lower etching current density to get macro-porous silicon layer MPSL at low anodization duration. For this study, photo-assisted electrochemical etching technique was used to create a porous layer on n- type surface wafer silicon. Such an obtained porous layer was investigated by means of x-ray diffraction (XRD), optical microscope (OM), and Fourier transform infrared absorption (FTIR).

Experimental

Samples of Si (111) orientation of about 12 Ω.cm are cut from n-type (1×1 cm^2) was used to prepare PSL. Methanol and alcohol are used commonly to clean the wafer in the ultrasonic bath for few minutes. Finally, they are rinsed in distilled water treated ultrasonically followed by drying in a hot air stream. PSL etching was performed in 40% HF: 99.9% ethanol solution (1:1) volume ratio in photo assisted (diode laser 40mw-650 nm) at room temperature. PECE is carried out at three different values of etching time t = 2, 3 and 4 min. For the electrochemical etching process, a constant current density of J=5mA/cm^2.we used same set-up presented in [6]. To ensure as uniform a current distribution as possible, ohmic contacts on bulk silicon were made by deposition of high purity Al films by using thermal resistive technique under vacuum pressure of 10^{-6} torr. After evaporation process, thickness of evaporated film on a glass substrate was measured using gravimetric method and was about of 1μm.Optical microscopy pictures for topography study are recorded by an INNOVATIVE DIGITAL MICROSCOPE 3.6MP.4.3 inch LCD. Surface chemical

composition of samples is best probed with Fourier Transform Infrared (FTIR) spectroscopy, The (Shimadzu-IRAffinity-1) scans of the FTIR measurements are performed over range between (400-4000)cm^{-1} for prepared sample. The crystalline structure of the experimental samples was investigated by a X-ray device (shimadzu - XRD6000) supplied from Shimadzu Company /Japan. The source of X-ray radiation has been Cu-Kα radiation with 0.15406 nm wavelength. The device has been operated at 40 KV and 30 mA emission current. Thickness and porosity of the prepared PSL are measured by the gravimetric method, a Mettler AE-160 digital with accuracy of 10^{-4} gm is used to weight the samples.

Results and Discussion

Fig. 1 shows the surface images of porous silicon / bulk silicon interface cross-section in Fig. 1(A) and porous silicon layers which were prepared in 2,3-4min etching time in Fig. 1 (B, C-D) respectively. A new phase in the surface topography of porous silicon layer we can observe in Fig. 1, the mud-like structure of PSL is a typical sample of cracking pattern and the effect of anodization duration on the shape and size of separated cracks in the porous silicon layer was clear in Fig. 1 (B, C-D). Crack formation as a result of increased etching time agree with Bisi et al., reported that the origin of the cracking is the large capillary stress associated with the evaporation from the pores [4]. Also that agree with Wali, reported that the widening of the cracks and increase their number are related to the increasing of etching time [7].
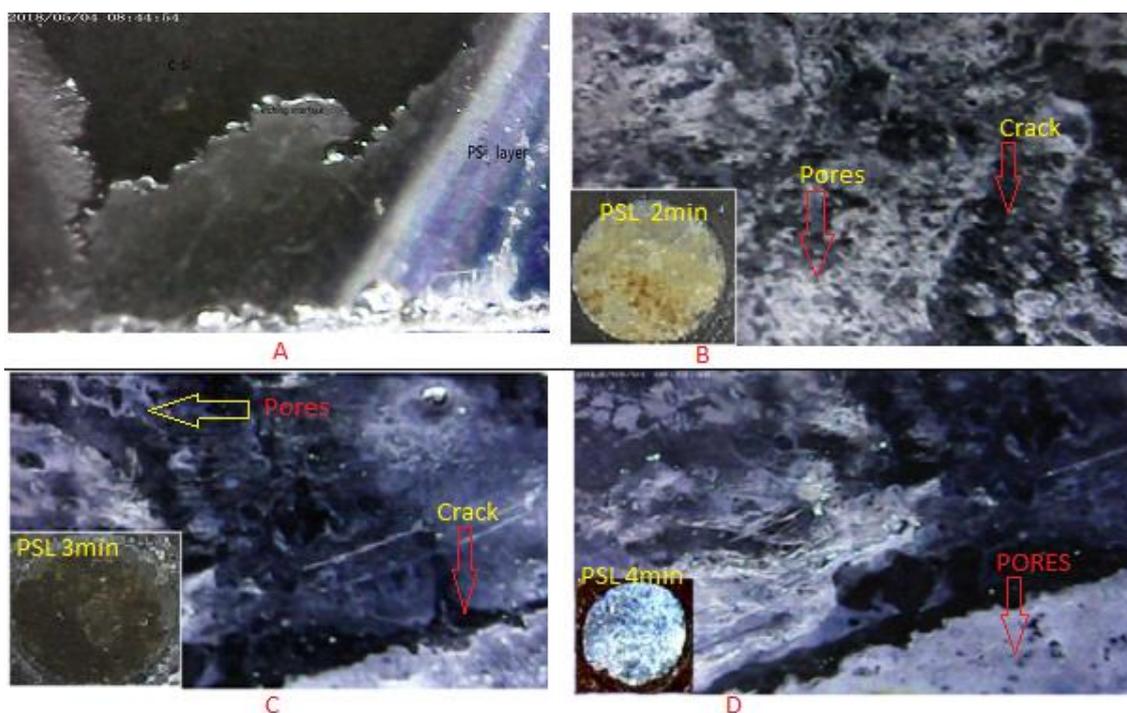

Figure 1. High resolution optical microscopy image of mud-PSL at different etching time (A: Interface c-Si/PSL, B: at 2 min, C: at 3 min, and D: at 4 min).

Porosity is gravimetric measurement: m_1 the mass of the wafer silicon before anodization, m_2 the mass of the wafer silicon after anodization and m_3 the mass of PSL after a rapid dissolution of the whole porous layer in a NaOH solution. The porosity P, thickness T and etching or growth rate r_p are given by the following equation [4, 8].

$$P\% = \frac{m_1 - m_2}{m_1 - m_3} \qquad (1)$$

$$T = \frac{m_1 - m_2}{\rho * A} \qquad (2)$$

where $m_1 - m_2$ is the weight of the sample in gm, A the area of the sample in cm^2 and ρ the material density in gm.cm^{-3}. Through the depend of the etching process of the silicon structure and create pores with etching time, we have shown that in Fig. 2, the increase of porosity and thickness of the porous layer with etching time from 2 to 4 min as illustrated in Table 1. That agrees with Fodora et al. reported that the average porosity increases rapidly with thickness silicon [9].
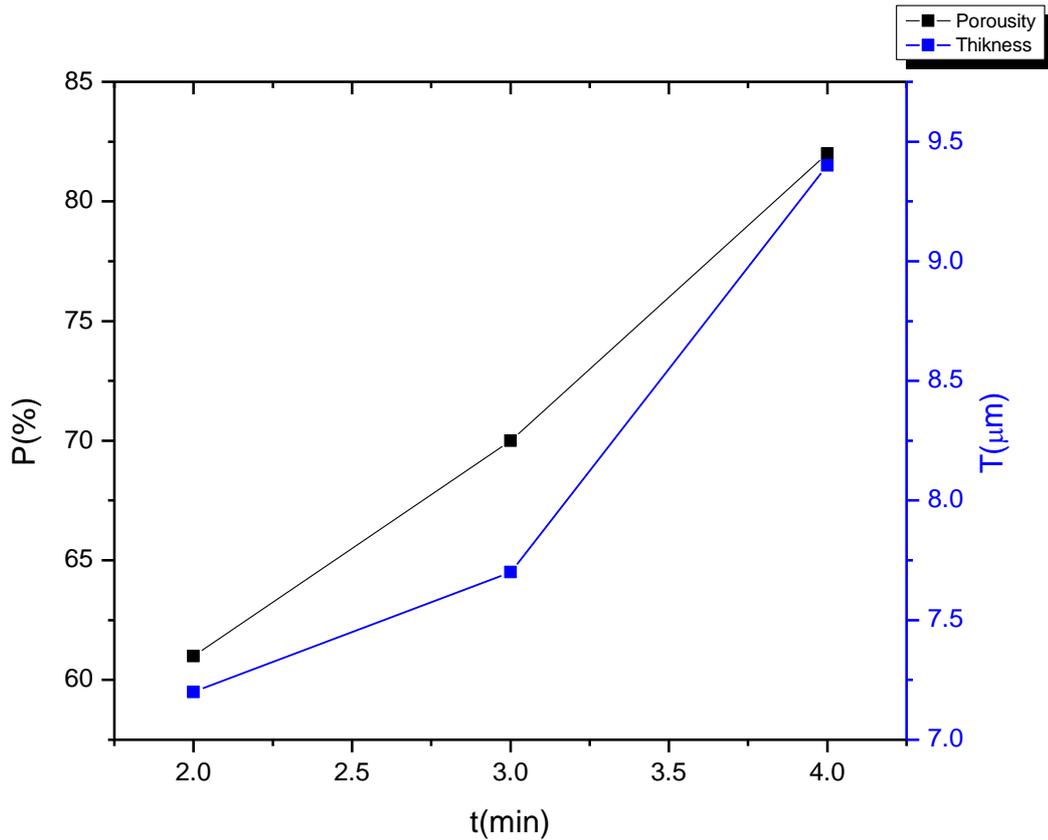
Figure 2. Porosity and thickness vs. etching time (t) of the PS samples.

Etching rate or growth rate data of the porous silicon measured by Eq. 3. The thickness T and thereby the growth rate r_p. The decrease of etching (growth) rate is correlated to the decrease of the porosity and thickness as shown in Fig. 3.

$$r_p = \frac{T}{t} \qquad (3)$$
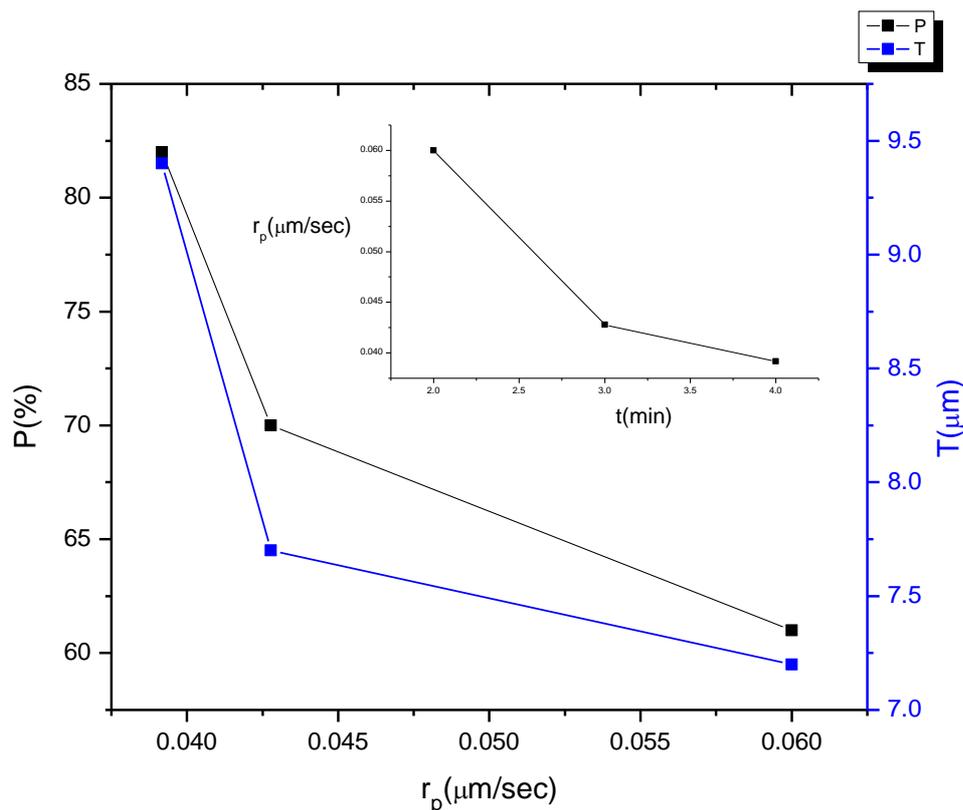
Figure 3. Calculated values of porosity and thickness as a function of the growth rate and inset the relation between etching rate and etching time.

Table 1 summarizes the calculated values of porosity, thickness and growth rate as a function of the Etching time.

Table 1. The values of porosity, thickness and growth rate.

Etching current density		5mA/cm^2	
Etching time(t) (min)	Porosity(P) (%)	Thickness(T) (μm)	Etching rate(r_p) (μm/sec)
4	82	9.4	0.039167
3	70	7.7	0.042778
2	61	7.2	0.06

The x-ray diffraction patterns of the bulk silicon (n-type) and PSL for 2, 3, and 4min anodization time are illustrated in Fig. 4 which show that one diffraction peak and has high intensity appearing at 2θ about 69.4° for c-Si and two diffraction peaks (primary and secondary) have been low intensity at 2θ about of 69.45° -69.67°, 69.39°-69.58°, and 69.45°-69.65 °respectively for PSL at 2, 3, and 4 min anodization time. The low intensity and broadening of XRD from PSL are due nanostructure layer of porous silicon was formed and it is clear that the effect of etching time on a position and the broadening peak of PSL. The peaks are indexed (as summarized in Table 2) near to 69.39°-69.45° (400) $_{PLS}$ reflection according to international center for diffraction data (2011) and JCPDS (1997). The crystallite size L of porous silicon layer estimated by using Eq. (4).

$$L = \frac{K\lambda}{FWHM*cos\theta} \tag{4}$$

where λ is (0.15406 nm) of the Cu-Kα line, $FWHM$ is the full width at half maximum of the diffraction peak and θ is the diffraction angle. The crystallite size is listed in Table 2 and it was in the range of nm, therefore confirming the nanostructure of our PSLs and the crystallite size L is seen to decrease from with increasing etching time.
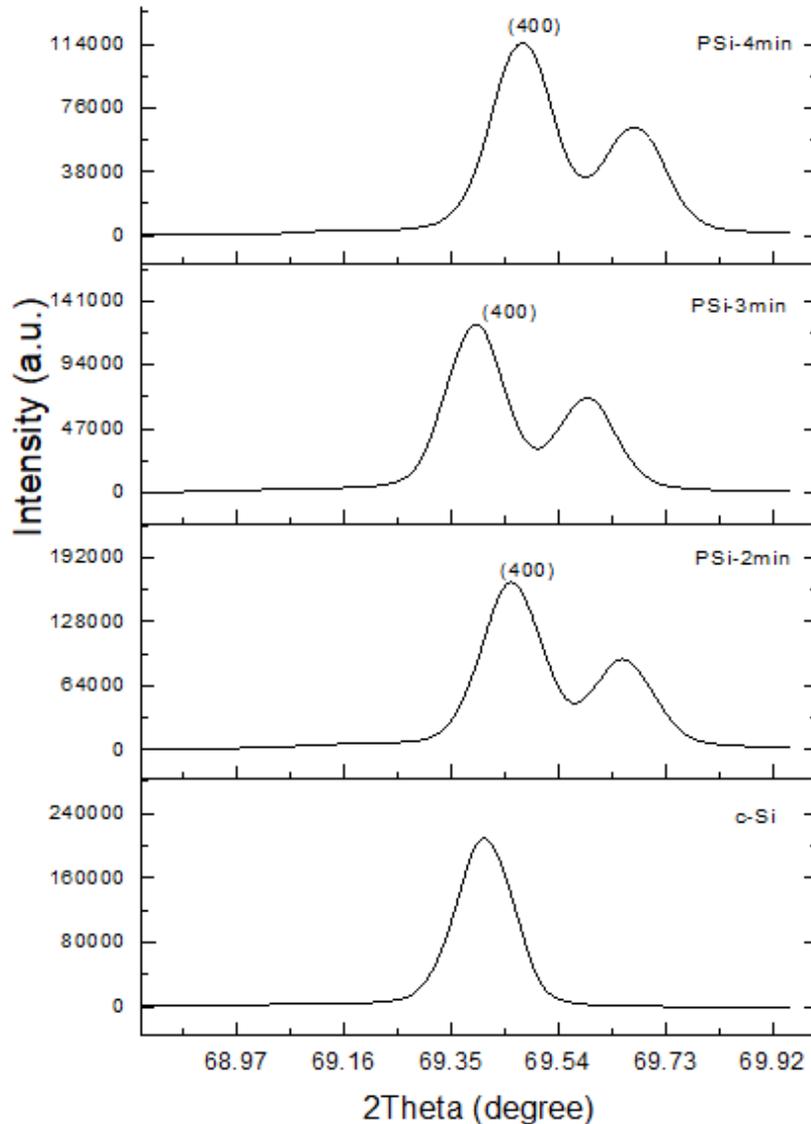
Figure 4. XRD pattern of c-Si and PSL prepared at 5mA/cm^2 etching current density and anodization duration 2, 3, and 4 min.

Most of defect is created in the interface nanostructures porous silicon-bulk silicon and the other defect is due to the other parameter such as strain. From Fig. 5, by increasing of etching time, the strain on porous silicon layer is increased and that correlated to increase of internal surface area. The strain induced by surface forces increases if the internal surface is enlarged [10]. Also, we can observe in Fig. 5, the nonuniform strain in the PSL at an etching time 3min due to the nonuniform behavior of the etching process. The nonuniform strain in the sample was evaluated using the Williamson-Hall method by Eq. (6) [11, 12].

$$\beta COS\theta = \frac{K\lambda}{L} + 2\xi sin\theta \tag{5}$$

where β is the peak broadening corrected for the systematic broadening in 2θ ; θ the diffraction angle; λ, the X-ray wave length; L, the crystallite size; and ξ, the nonuniform strain [12].

$$\xi = \frac{\beta COS\theta - K\lambda/L}{2 sin\theta} \tag{6}$$

Also, the crystal lattice strain ξ is evaluated from the lattice parameter changes between bulk silicon constant a_{Si} and porous silicon constant a_{PSi} by Eq. (7) and we have the same of result as presented in Table 2.

$$\xi = \frac{a_{Si} - a_{PSi}}{a_{PSi}} \tag{7}$$
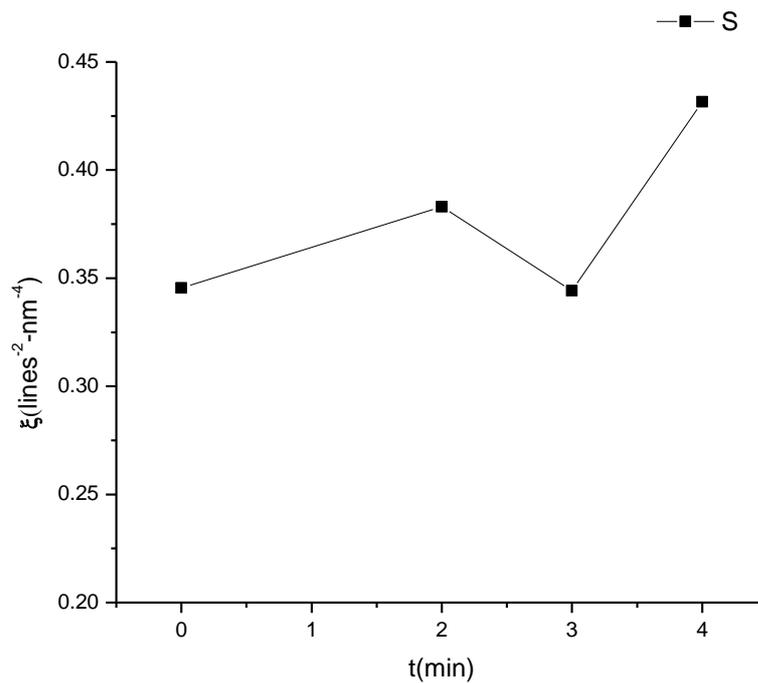
Figure 5. Crystal lattice strain ξ between the porous silicon and bulk silicon lattice constant as function of etching time t (min).

Fig. 6 shows that a good linear relationship between $\beta COS\theta$ and $2 sin\theta$ for all samples under anodization duration ,so that mean the effect of orientation on the peak broadening was negligible, the c-Si and PSL have been the same plane direction .
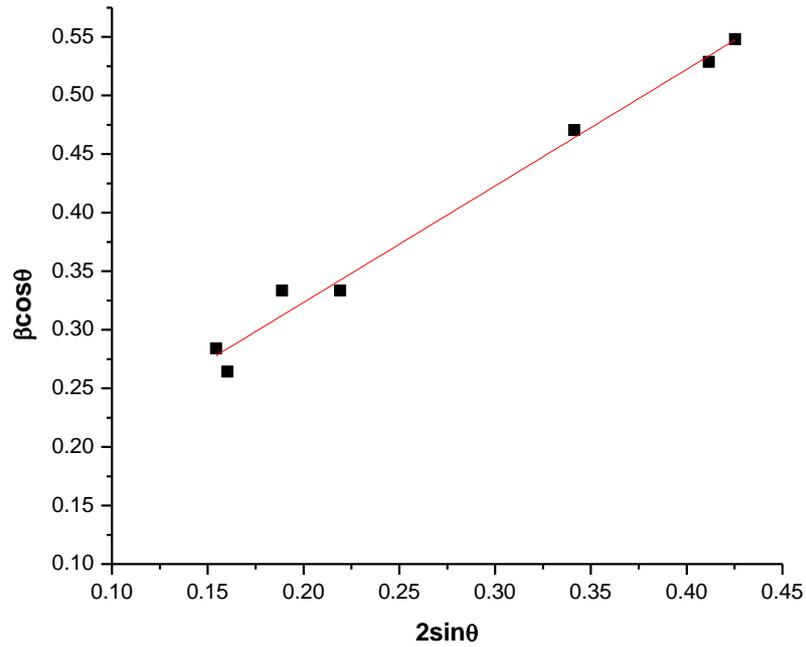
Figure 6. Relation between the peak broadening **βCOSθ** and **2sinθ** for all broadening (primary and secondary) peaks.

The dislocation density δ was calculated by using Eq. (8), where L is the crystalline size. Fig. 7 show that the dislocation density is increasing with increase etching time as illustrated in Table 2. The decreasing of crystalline size is supported that behavior for dislocation with etching time.

$$\delta = L^{-2} \tag{8}$$
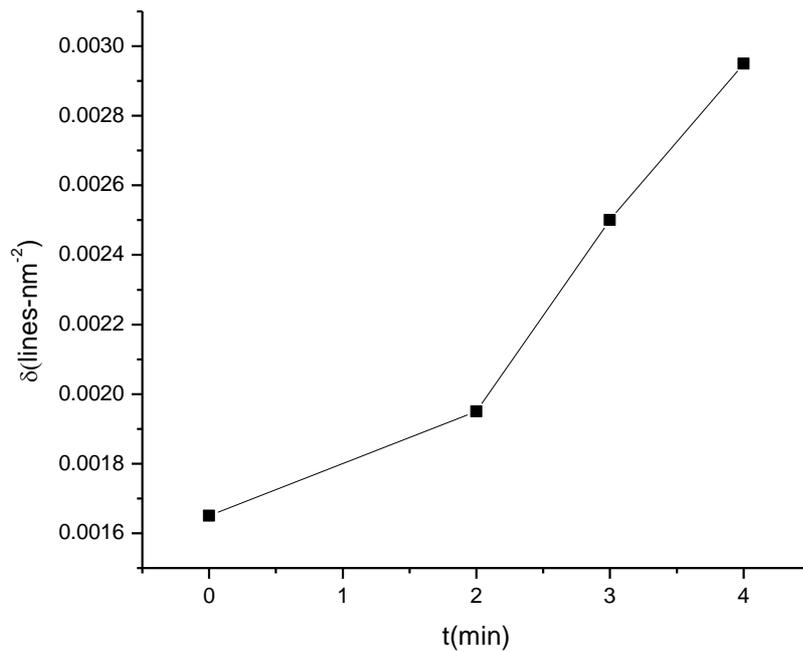
Figure 7. Calculated dislocation density verses different etching time.

Table 2. Crystal lattice strain (ξ), Dislocation density (δ), crystallite size (L), lattice constant (a) and Number of grains (N₀) for PSL sample as function of etching time.

Structure properties	PSL (2min)	PSL (3min)	PSL (4min)
2θ(deg)	69.45	69.38	69.45
d(A)	1.3523	1.3544	1.3516
FWHM(deg)	0.1112	0.1057	0.1132
$\beta\cos\theta$	0.188	0.128	0.219
L(nm)	22.65	19.99	18.42
$2\sin\theta$	0.333	0.264	0.333
a(A)	5.409	5.417	5.406
δ (lines-nm^{-2})	0.0019	0.0025	0.0029
ξ(Eq.7) (lines^{-2}-nm^{-4})	0.3830	0.3446	0.4316
ξ(Eq.6) (lines^{-2}-nm^{-4})	0.3830	0.3446	0.4316
N₀ (nm^{-2})	1.5E-06	9.6E-07	6.1E-07

Fig. 8 shows FTIR spectra of c-Si and freshly porous silicon layers prepared at 5mA/cm^2 current density for 2, 3 and 4 min anodization time from 400 to 4000 cm^{-1}. Most of the bands are observed and tentative assignments are shown in Table 3. The strong absorption feature in the wavenumber range of (1065-1085) cm^{-1} originates from asymmetric stretching of Si-O-Si. A change of the chemical structure of the porous silicon surfaces was observed for a longer etching time, the absorption peak was increased for some band and decreasing for other due to the anodization time in electrolyte chemistry as shown in Fig. 8. The characteristic bands shift toward a lower wave number region may be due to the increase in particle size with an etching time increase.
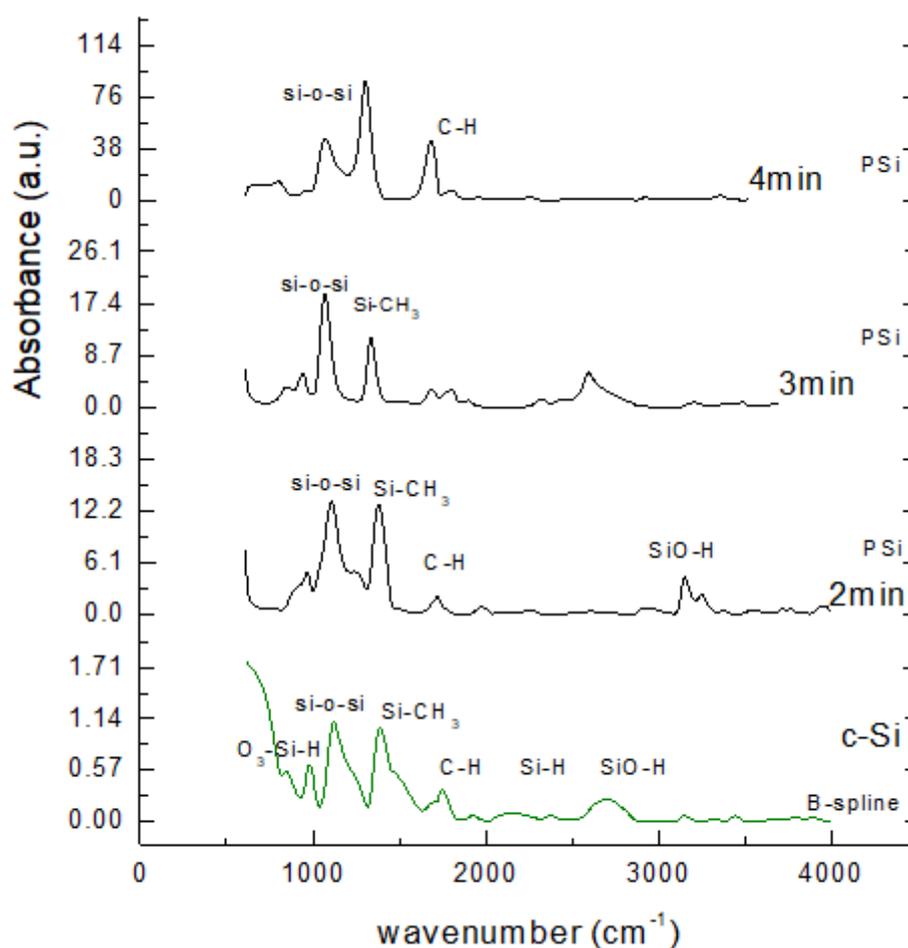
Figure 8. FTIR spectra of c-Si and PSL surface for 2, 3, and 4 min etching time.

Table 3. Surface bonding in the mud-PSL.

Peak (cm^{-1})	Attribution	Ref
1065-1085	Si-o-Si asymmetry stretch	[13] [14]
1463	CH_3 asymmetric deformation & C-H deformation	[14]
1380	Si-CH_3	[15]
3430	SiO-H stretch	[16] [14]
2080	Si-H	[17] [18] [13]
1720	Si-O Stretching in O-Si-O	[19]

Conclusion

Mud porous silicon was formed by photo-assist electrochemical etching at low etching current density. The OM images show that by increasing the etching time, the crack in the mud-like structure of porous silicon layers are widened. In addition, the intensity of PLS Bragg peak increases with the increasing of etching time. The change in the intensity of the PSL surface band is due to the anodization time in electrolyte chemistry.

Conflict of Interest

The authors declare that there is no conflict of interest.

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