Impact of Etching Time on Ideality Factor and Dynamic Resistance of Porous Silicon Prepared by Electrochemical Etching (ECE)

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Keywords: Porous Silicon; Electrochemical Etching; Ideality Factor; Dynamic Resistance

Abstract. In this work, porous silicon layers PS were fabricated on p-type crystalline silicon wafers using electrochemical etching ECE process. Al films were deposited onto porous layer /Si wafers by thermal evaporation to form rectifying junction. An investigation of the dependence on applied etching time to formed PS layer was studied. Effect etching time on the electrical properties of porous silicon is checked using Current–voltage I–V characteristics. The ideality factor and dynamic resistances are found to be large than the one and 20 (k Ω) respectively by the analysis of the dark I–V characteristics of Al/PS/p-Si heterojunction.

Introduction

Porous silicon composites provide modified functionality compared with as-prepared porous silicon and expand its applicability. The formation of porous silicon layers on crystalline Si wafers using electro-chemical etching ECE. Electro-chemical etching is one of the simplest and most reliable methods used to synthesis porous silicon PS [1-3]. Typically, the PS layer is sandwiched between the c-Si substrate and a metallic contact. The PS layer was considered to behave like a wide band gap semiconductor and assumed a Schottky barrier formed between the metal and the PS [4]. Nanostructured porous silicon PS was received on bulk Si wafers by the method of anodic electrochemical etching in hydrofluoric acid solution [5]. The most widely investigated device structure using PS layer is crystalline silicon metal/PS/c-Si [6]. The electrical characteristics of metal/PS/c-Si/metal structures have been shown to exhibit similar rectifying features irrespective of the metal used for top contacts. Therefore, transport of carriers within the PS layer thickness and across the c-Si/PS hetero-junction governs the device characteristics [7]. Porous silicon photo-conductors are commonly fabricated by depositing aluminum film on top of oxidized porous silicon structure. The passivation of the surface by oxidation could improve the external quantum efficiency of porous silicon photo-diode [8]. The practical applications are oriented towards the fabrication of new structures and devices. The compatibility of the nano-crystalline silicon-based materials with the classic mono and/or polycrystalline silicon (bulk or thin films) permits the use of these new materials for the integrated micro and optoelectronics, photonic crystals, bio-medical applications or efficient sensors [9]. To study the PS/c-Si junction properties, I-V measurements, usually, provide a valuable source of information about the junction properties. In general, the electrical properties of the Schottky contacts on n-Si type, p-Si type and the other semiconductor have been investigated by large number of research groups by different method [10]. Analysis of current–voltage I–V characteristics of Al/PS Schottky junction allows us to understand different aspects of current transport. For an ideal Schottky diode, the current flow is only due to thermionic emission mechanism and the ideality factor should be equal to unity. However, due to various factors such as device temperature, dopant concentration, device area, density of interface states, structural properties of interface etc. [11]. In this work, Al films were deposited onto porous layer /Si wafers by thermal evaporation to form rectifying junctions. The electrical properties of the junctions were determined by current-voltage I-V. In this paper, we present an effect etching time on I-V measurement of Al/PS/p-Si devices and influence that on the ideality factor and dynamic resistance.

Experimental and setup

The fabrication of Porous Silicon is a comparatively simple process that only requires a small amount of equipment. The simplest cell which can be used to anodize silicon is shown in Fig. 1.

Figure 1. Schematic of the designed porous silicon fabrication system.

The silicon wafer serves as the anode. The cathode is made of platinum or any HF-resistant and conducting material. The cell body itself is, in general, made of highly acid-resistant polymer such as Teflon. Since the entire silicon wafer serves as the anode, PS is formed on any wafer surface in contact with the HF solution, including the cleaved edges. The advantage of such equipment is its simplicity [12]. The main element of the system as shown electro-chemical cell. We used this method to prepare PS from p-type as shown in the following sections. Porous silicon layers are produced using mono-crystalline silicon wafers, p-type and n-type, with resistivity's ranging from 14-22 ($\Omega\cdot\text{cm}$) for p-type and 10 ($\Omega\cdot\text{cm}$) for n-type. The wafers Si (111) face orientation. Samples are made of porous silicon produced with a standard technique of anodizing either n- or p-type silicon substrates in an electrolyte 40% HF:99.8% CH_3OH with a volume ratio of [1:1]. The Si wafer first cuts to $1\times 1\text{ cm}^2$ samples before cleaning. Cleaning is necessary to remove any traces of organic, metallic and ionic contaminants from samples. Methanol and alcohol are used commonly to clean the wafer by immersing it in these chemicals in turn in the ultrasonic bath for few minutes. Finally, they are rinsed in distilled water treated ultrasonically followed by drying in a hot airstream. To ensure as uniform a current distribution as possible, the samples are coated with $\approx 800\text{ (nm)}$ layer of aluminum on the backside. The samples are prepared in sandwich configuration, top Al/PS/c-Si/bottom Al, the top one Al semi-transparent electrode thermally evaporated thin layer. The rear-side ohmic contacts were fabricated by the electro-chemical deposition of thick Al film to get sandwich structure. The samples are prepared in sandwich configuration, top Al/PS/c-Si/bottom Al, the top one semitransparent electrode thermally evaporated with 78nm and the bottom electrode is coated with $\sim 800\text{ (nm)}$ Aluminum layer before the anodization process. Porous silicon samples are prepared by anodization in HF: and CH_3OH (1:1) solution at a constant current density values within the range from 20-60 (mA/cm^2) for different times to any value of current density 5-30 (min) at room temperature. Metallization on PS has also become another important area of interest, especially in the Schottky diode structure. The success of PS in the application areas depends on how the big challenge in seeking suitable metallization can be overcome [13]. The evaporation is performed in a vacuum pressure of 10^{-6} (torr), using an evaporation plant model "E306 A manufactured by Edwards high vacuum". After the evaporation process, the thickness of evaporated film on a glass substrate is measured using gravimetric method. Measurement is achieved in department of Physics in College of Sciences / Baghdad University. The thickness measurement by gravimetric method is carried out using the equation:

$$m=2\rho\pi l^2t \quad (1)$$

where m is the net mass of evaporated Al on glass substrate, $\rho=2.7(\text{g. cm}^{-3})$ and $l=15(\text{cm})$ the distance between the boat and substrate. Dark current – voltage in forward and reverse directions Sn/PS/c-Si/Al measurements are carried out by applying voltage supplied to the sample from stabilized d. c. Power supply, type LONG WEI DC PS-305D 30 ranges -10 to +10 (V). The current passing through the device is measured using UNI-T UT61E Digital Multimeters.

Results and discussion

The dark I–V characteristics at different etching density current in the current range of 20–60 (mA/cm^2) for the PS/p-Si hetero-junction, also at different etching time range of 5-30 (min) are shown in figures 2-6. Figures 2-6 shows the current – voltage (dc) measurements that are made in the dark on a number of samples of Al/PS/p-Si/Al structures. A linear behavior in the semi-logarithmic plot enabling, one to extract the important diode parameters (ideality factor n). The I-V characteristics of the junction in the figures 2-6 can be explained as in the following observations; nonlinear behavior: (at low voltages), that's mean under the forward bias condition; it shows the exponential increase in current due to decrease in the depletion layer width at the PS/c-Si interfaces. Under reverse bias, for all cases, it is clear that the curves contain two regions; in the reverse bias and at the same values of the voltage, reverse current is slightly increased with the applied voltage and this leads to generate electron- hole pairs at low bias (for zero applied voltage exactly balances the diffusion current). The depletion layer width increases and the current is due to the minority carriers of PS dependent on voltage applied. In this case, the current results from the diffusion of minority carriers through the junction. The enhancement in the reverse current is related to enhancement in the junction structure, which results in reducing the number of defects at PS/c-Si interfaces of the junction. These defects result from the strain due to crystal structure. The PS layer thickness and PS/c-Si interface are not monotonically proportional to the etching current density time and etching time. Linear behavior: (at higher voltages) the current-voltage characteristics are almost linear because the depletion layer is minimized at the Al/PS/c-Si/Al interfaces and PS act as series resistance. In the forward bias, majority carriers are able to cross the potential barrier much easier than at low voltage bias which results in reducing the height of the potential barrier, so that the diffusion current becomes greater than the drift current. Most the diodes are of the $\text{contact}_1/\text{PS}/\text{Si}/\text{contact}_2$ structure, for which the $\text{contact}_2/\text{Si}$ junction is designed to be Ohmic and of negligible series resistance, i.e. it has no bearing upon the I-V characteristics. For this reason, contact_2 , in the case of silicon, one can simply deposit a metal such as aluminum and obtain a reasonable Ohmic contact. This is usually Al [14]. Rectification behavior: In the exponential region, according to the usual junction rectification models. The relation between the current and the applied voltage can be written as Eq.2.

$$I = I_0 \left[\exp \left(\frac{qV}{nKT} \right) - 1 \right] \quad (2)$$

where, I_0 is the reverse saturation current and is given as:

$$I_0 = A^* T^2 \exp \left(\frac{-q\phi_b}{nKT} \right) \quad (3)$$

where A^* Richardson constant, n the value of ideality factor, V is the applied voltage and T is the temperature in Kelvin. The ideality factor of Al/PS/c-Si/Al surface type Schottky diode is calculated from the current-voltage characteristics by using the following Eq. [15]:

$$n = \frac{q}{KT} \left(\frac{dV}{d \ln I} \right) \quad (4)$$

The dark current is decreasing with increasing etching time from 5-40 (min) at the same bias voltage. As shown in almost the figures (An exception is the behavior at 30 (min) etching time in $> 20(\text{mA/cm}^2)$), that agree with the dependence of dynamic resistance on etching time; increasing

the etching time (increasing porosity) leads to higher resistance in ($K\Omega$) as shown in figures 2-6. The PS samples etched for different time and current density exhibit distinct difference of the forward current when these devices are operated under same external bias, as the figures show. When the devices are operated at 30, 40 and 60 (mA/cm^2) current density, the current of the sample etched in 30 (min) shows small decrease of the current compared with that of the samples etched for others time. The current variation of the sample etched for 30 (min) is large, but the current variation of the others devices show small change of the forward current when the devices were operated at 20 and 50 ($\frac{\text{mA}}{\text{cm}^2}$) at the same external bias for all devices. At this point there are many reported trying to illustrate the mechanism governing the current transport process through PS structures. Palma reported that the presence of a large concentration of interface states controlled the current of the devices [16]. The metal-porous silicon barrier played a significant role in the transport mechanisms [17]. The total current of devices was governed by carrier transport in the high resistivity PS layers [18]. We can say that most of the model used to explain many cases, up to etching condition, structure properties, Schottky properties, and type of substrate. Soft breakdown is observed under reverse biasing condition. The rectifying behavior is attributed to the difference in junction area and Schottky barrier height of the dominant junction (Al/PS, PS/p-Si, and p-Si/Al) for p-type. At last, according the first and second point, we have two regions; the first one recombination center region at low voltage and tunneling region in the interface junction at high voltage. Third point can classify that the type of the junction is anisotype junction. Also other points show the forward current decreases with increasing etching time, when etching time increases the porous layer increases and the porosity increases, so the pore walls act as carrier trapped and cause high resistivity.

Figure 2. I -V curves of an Al/PS/p-Si/Al structure at 20 (mA/cm^2) with different etching time.

Figure 3. I -V curves of an Al/PS/p-Si/Al structure at 30 mA/cm^2 with different etching time.

Figure 4. I –V curves of an Al/PS/p-Si/Al structure at $40 \text{ (mA/cm}^2)$ with different etching time.

Figure 5. I –V curves of an Al/PS/p-Si/Al structure at $50 \text{ (mA/cm}^2\text{)}$ with different etching time.

Figure 6. I –V curves of an Al/PS/p-Si/Al structure at $60 \text{ (mA/cm}^2\text{)}$ with different etching time.

In the Fig. 7 the resistance of the sample variance within the limits of 20-1000 (k Ω) for p-type. Also, this result is in a good agreement with our result in I-V measurement. The increasing of the thickness increases the dynamic resistance of the junction. This can be explained as the smaller current densities pass within the porous structure, although the PS layer has a higher dynamic resistance compared with those for low dynamic resistance PS layer as shown in the behavior of I-V characteristic.

The ideality factor gives the deviation of the diode characteristic from that of the ideal diode. The values of n obtained for the Al/PS/c-Si/Al structure is found to be from 2.69 -19.9 at voltages ranging $\Delta V = 0.2 \text{ (V)}$ as shown in Fig. 8 for p-type. The high ideality factor can be attributed to the sum of the ideality factors of the individual rectifying junctions (i.e., the actual PS/c-Si heterojunction junction and Schottky diodes at the Al/PS or the two metal-semiconductor junctions (Al/PS, c-Si/Al) of a diode ideally have Ohmic characteristics). When the structure has a series resistance and interface states, ideality factor n becomes higher than unity; most practical Schottky diodes shows deviation from the ideal thermionic theory. The fact that such recombination currents

are flowing not homogeneous in the structure, but always at local sites, e.g. in extended defects, affect etching time on the crystalline size and strain. It agrees with the large ideality factor which is attributed to the roughness of the PS surface. The large lattice mismatch of PS and c-Si approximately at the same etching time all the values of ideality factor n decrease with increase current density, also at constant current density, the ideality factor n has the same behavior when increasing etching time. That means inhomogeneous structure leads to getting high n ideality factor. The high of density of trap states. These traps are responsible for the recombination of the electron-holes generated because of the application of relatively generous higher biasing voltage. The presence of nonlinear metal-semiconductor contact. An ideality factor, $n > 1$, is commonly used to phenomenological model the non-ideal characteristics (with $n=1$ for the pure thermionic emission case) [19]. Interfacial oxide layer may also be the possible cause for a higher ideality factor [20].

Figure 7. Dynamic resistances of p-PS as function of etching time.

Figure 8. The variations in the ideality factor of the J-V curves as a function of etching time.

Conclusions

In this work the preparation of nano-crystalline porous silicon by electrochemical anodization has been described. Electrical properties of porous silicon have been mentioned. The results show that the ideality factors for junctions indicating that this sample can show a good Schottky behavior. The ideality factor and dynamic resistance of porous silicon are found strongly dependence on etching time. The device shows a non-ideal current-voltage behavior due to the ideality factor being higher than unity and that agrees with the dependence of dynamic resistance on etching time.

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